

MOSFETs modeling using artificial neural network

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Abstract

The invention of the transistor in 1948 launched a real technological revolution that continues today there are two families of transistors responding to different operating principles: the bipolar transistors invented in 1948. But they are considered as an old technology. A type of transistors derived the field effect transistors (MOSFET), dominate today and more useful than the bipolar. The current technology needs an intelligence technique, modeling of electronic components by artificial neural network. Our work within this framework, as it presents to us a first step in exploiting the principles fantastic techniques of artificial intelligence in the field of modeling and simulation of electronic components such as MOSFETs.

Keywords: MOSFETs, Artificial Neural Networks, Modeling .

1. Introduction

Electronic devices nowadays have considerable economic and strategic importance. They play an increasingly key role in the implementation and operation of a large number of consumer goods. Their importance was born with the discovery of the transistor, the concept dates back to 1930[1]. The development of the microelectronics industry has accelerated the manufacturing of integrated circuits. Over the years, the microelectronics industry has focused on three objectives to ensure its growth: 1) miniaturization of electronic components, 2) fast execution and 3) cheaper design [2]. The MOS transistor (Metal- Oxide - Semiconductor) is an important device. So far, the reduction of MOSFET dimensions was carried out continuously and very fast, this rapid technological change is largely due to the increased control of silicon technologies, semiconductor constituting the heart of the MOS devices. However, these devices have to be mastered by IC designers, and need to be modeled in the form of compact models able to describe as accurately as possible the electrical behavior of these devices. The simulation of microelectronic components therefore needs new theories and modeling techniques (such as artificial intelligence techniques), to improve the physical understanding of micro and nano - sized devices [3, 4]. The field of modeling and simulation of microelectronic components can be considered as an important field of applications of the techniques of artificial intelligence. Therefore, the study of the possible use of artificial neural networks in the field of microelectronics, such as preachers and simulators components (MOSFETs) is necessary [5, 6]. This work

falls within this framework, because it presents to us a step in the operation fantastic technical principles of artificial intelligence in the field of modeling and simulation of electronic components such as MOSFETs.

2. Field effect transistors MOSFETs

The FETs (Field Effect Transistor), are active electronic devices whose conduction state and the current intensity are controlled by the voltage applied to a distinct electrode called the gate [7]. It is a wide variety of FET; the JFET (Junction of Field Effect Transistors), where the gate voltage control the extension of the depletion region of a PN junction (the channel), MESFET in which the PN junction is replaced by a metal - semiconductor junction, and finally the MOSFET wherein the gate is separated from the semiconductor by an oxide (mostly by SiO₂), playing the role of an insulator[4]. We are particularly on the silicon MOSFETs were then gradually replaced bipolar transistors and even JFET transistors with their fantastic features in many applications. A comparison between the electrical characteristics of the JFET and MOSFET. By principle of the control of the conducting state by a voltage [5]. And in addition the MOSFET is used today in many applications, for which the requirements in terms of performance of the components are not all the same. Also, there is no for each technology node a single MOSFET that would be used in all existing circuits [8].

3. Device structure and physical operation

3.1. Device structure

Figure 1 shows the internal structure of a MOSFET N - channel enhancement. Typical dimensions of a MOSFET:

- a channel length of MOSFET L is 0.1 to 10 microns.
- The thickness of the oxide layer 2 to 50 nm,
- Width (transistor width) of 0.2 to 100 microns.

N - channel enhancement

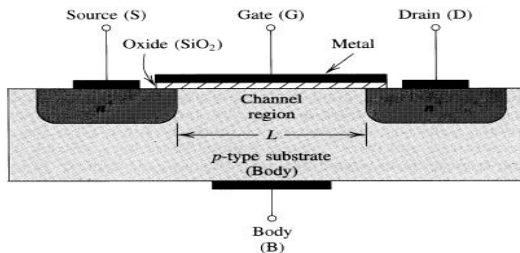


Figure 1. The internal structure of a MOSFET N - channel

In the latest integrated circuit technology, the channel length can be reduced to 45 nm (short - channel MOSFET) [9].

3.2. Operation of an enhancement N-channel MOSFET

Suppose that no voltage is applied to the gate and a small potential difference $V_{DS} = V_D - V_S$ ($V_{DS} > 0$) is applied between the drain and source. In this case, the MOSFET be considered as two PN junctions placed in opposition: a first between the drain and the substrate, and a second between the substrate and the source. These junctions are at best through which a leakage current in low definition. The drain current I_D then be nil [10, 11]. To allow a current to flow from the drain source, create a conductive channel, as shown in figure 2. For this, a voltage is applied to positive grid relative to the source, which has two effects:

a - First, this voltage repels holes, which are majority carriers of the substrate, which creates a depletion region directly below the gate.

b - In a second step, a positive voltage V_G attracts below the gate electrons. When the density is sufficient, they form what is called an inversion layer (the S / C becomes N-type), the conduction channel. These electrons come from either the heat generation in the volume of the substrate, either directly from the N + regions of the drain and the source. After formation under the gate channel, applying a slight tension between the drain and the source generates I_{DS} drain current flowing to the source. Thus, taking the source voltage V_S as a reference point, a channel is created for a V_{GS} voltage higher than a threshold voltage V_T , typically a few volts [12, 13].

3.3. Output characteristic NMOSFETs

To understand the behavior of the nMOS, start by analyzing the output characteristic.

-Curve describing the electrical behavior of the transistor in the plan: (I_D , V_{DS})

- I_D = Drain current = current through the transistor drain.

Figure 2: The graphic representation of the dependence between I_D and V_{GS} .

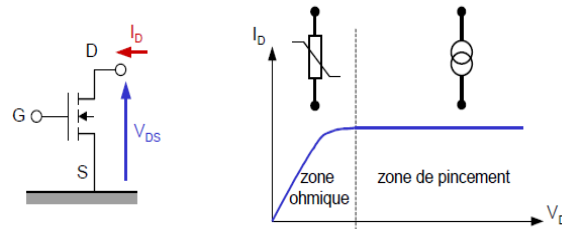


Figure 2. The graphic representation of the dependence between I_D and V_{GS}

3.4. Modelling using Artificial Neural Networks

The structure we have adopted is a network that correspond to the two input voltages V_{GS} and V_{DS} , two hidden layers of neurons 10 and 5, respectively, and one output that corresponds to the output current of the transistor I_{DS} (the drain- source). This structure is illustrated in Fig. 3 below [3, 14].

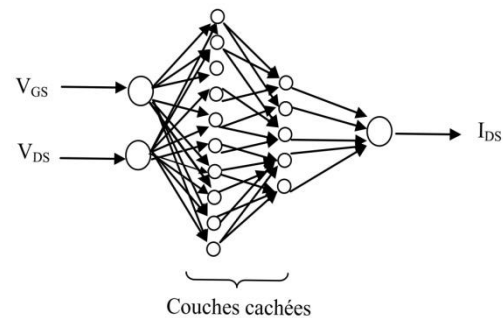


Figure 3. Structure of the network used

3.5. Network Training

The values which set in this stage: for V_{DS} : of 0V in 15V by step of 0.5V and for V_{GS} V the transistors support many tensions are more important, but one limited itself to this rand of V_{GS} and V_{DS} to minimize the time of training. Finally the training of both networks is made after 150.000 iterations. The results which we obtained are illustrated in Fig.4.

Two curves represent the characteristics $I_{DS} = F(V_{DS})$ stemming from the theoretical and the neuronal model. The X axis presented the couples of inputs of learning V_{GSi} and V_{DSi} . We notice that both models are identical, and do get small errors which near it means that the parameters of the network adopted are good. We have found that the theoretical and neuronal model is almost identical either for the typical first one of transistor.

3.6. Validation of network

The operation of network validation consists its test by the input data which used to its learning. This operation is consequently a first assesment of the efficiency of the mechanism of training. The data which used during: V_{DS} : (0V in 15V) by step of 0.5V and V_{GS} (0V in 10V) by step of 0.5V the results which we obtained are illustrated in Fig.4.

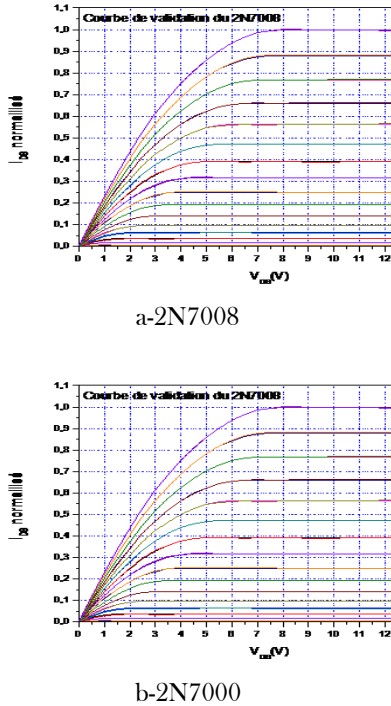


Figure 4. Characteristics $I_{DS} = F(V_{DS})$ of 2N7008/2N7000 estimated and theoretical

The 2N7008 and 2N7000 characteristics $I_{DS} = F(V_{DS})$ and estimated are drawn from the data of the validation. We can say that curves are closed for the various values of V_{GS} and we want to say the obtained model reproduced faithfully the static characteristic of the MOSFETs.

3.7. Test of network

The test itself of the network, consists in excited the weighty structure and on the bias obtained after the phase of learning by couples of inputs other than those who were of used during the training. This operation represents the assesment of the efficiency of the process of training. In our case we used the following vectors of test: V_{DS} (2.25 - 6.25) by step of 0.5V and V_{GS} (5.1 in 7) by step of 0.1V. The obtained results (profits) are represented on the following curves:

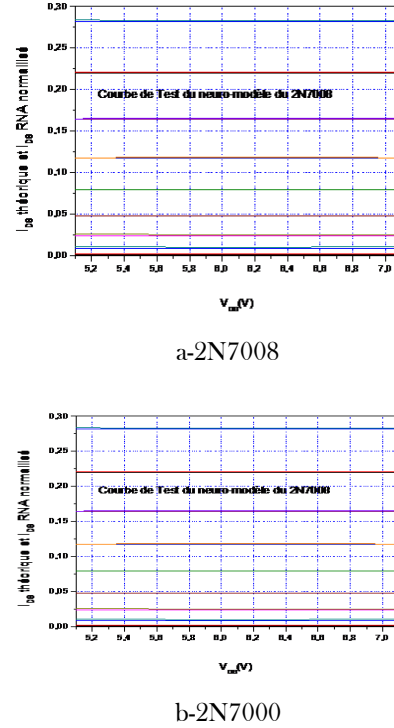


Figure 5. Characteristics $I_{DS} = F(V_{DS})$ of 2N7008/2N7000 of test

4. Results and discussion

We notice in both cases, for the 2N7000 or for the 2N7008 that curves are almost identical. It naturally reflected the good quality of the weights and the biases of the neuronal structure which we obtained. These results are in agreement with what was found by Shastrakar et al[15]. For more details, we represent the samples of results taken to visualize better the error between the results obtained in theory and by the test results of the network in other side.

Both figures represent samples of curves pulled from the curves. The choice of these samples for both types of transistors summer at random because for all the values of V_{GS} take snuff during the test, both models are almost

identical to error near and which are as we can even on these very weak curves of the order of 10^{-3} .

In this part of this work we are going to place the models neuronal which we conceived in circuits useful for transistors MOSFETs taken from the literature [16].

The first assembly rose around one 2N7008, and the second is an assembly with transistor 2N7000.

All the couples VDS, IDS can take the currents and the tensions of the transistor implanted in this circuit the plan of the right of static load responsibility of a circuit is very important, because she helps to know the location of the point of functioning in other literature of rest of the transistor[17,18].

The obtained curves show a very big similarity between the results obtained by calculation or by prediction from the model neuronal. It is shown with certainty on both figures.

Indeed in remark that as for the currents, the tensions obtained by both approaches are identical and it can be seen by the slopes of the curves which are equal to the unity.

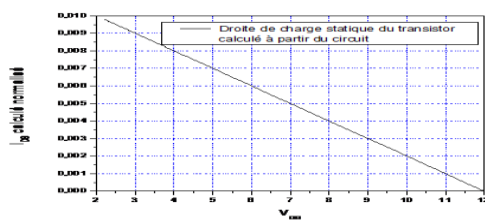


Figure10. The load line circuit theory Traced

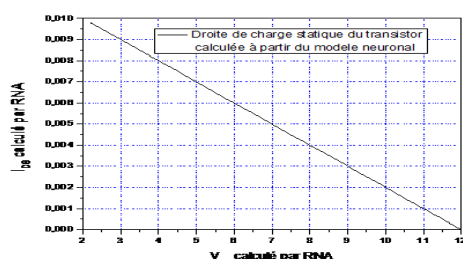


Figure 11. The load line circuit predicted by ANN

5. Conclusion

The purpose which we drew at the beginning of our work is to realize a model with artificial network of neuron of a transistor MOSFET with canal N in enrichment. This model had to predict the behavior of this very important electronic component in the modern manufacturing of integrated circuits, when it is placed in useful circuits. In the end we followed logical stages which led us directly to our purpose. The results which we obtained were very good and both models predict converged quickly and effectively on the theoretical formalism obtained the current drains sources of both transistors, what is shown well by the weak error obtained after the various operations of test.

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