

Study of different parameters effects on threshold voltage of CNTFET

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Abstract

In this paper, we have studied the effect of different parameters on threshold voltage of CNTFET devices using a numerical model developed with the Non-Equilibrium Greens Function approach in real space. In fact, the work in hand involves the V_{TH} as a function of length gate taken from 10 nm to 30 nm for different temperature namely : 77 K, 150 K, 300 K, 400 K. then the variation of V_{TH} as a function of the nanotube diameter varying over the following chiralities : (13, 0), (16, 0), (19, 0), (23, 0), (25, 0) was undertaken. Afterwards, we conducted the variation of V_{TH} as a function of the oxide thickness with the values: 1.5 nm, 3 nm, 4.5 nm, 6 nm and 7 nm. Moreover, the V_{TH} was carried at depending upon the high-k materials such as: SiO_2 , HfO_2 , ZrO_2 , Ta_2O_5 and TiO_2 . And the source/drain doping used are 2.5 m^{-1} , 4 m^{-1} , 6 m^{-1} , 8 m^{-1} , and 10 m^{-1} (~ 0.01 dopant/atom). Finally, a conclusion is made basing at the different findings which revealed that the best reduce of V_{TH} was recorded under a liquid Nitrogen temperature of 77 K.

Keywords: CNTFET; Nano-transistor; Threshold voltage; NEGF method.

1. Introduction

MOSFET (metal oxide semiconductor field effect transistor) has become one of the most important semiconductor devices today for VLSI chips. The theme of semiconductor technology is to scale down the size of transistor and to increase the integration of transistor in a single chip. Advanced semiconductor devices have been scaled down to nanometer level, and the device sizes are continually shrunk as predicted by Moore's law [1].

The short channel effects, threshold voltage roll-off, drain induced barrier lowering, and band to band tunneling have become increasingly significant as the channel length of semiconductor devices has gone down the deep nanometer level [2]. High-performance FETs have been demonstrated based on carbon Nanotube (CNTs) or 2-dimensional (2D) graphene because of macromolecular systems with unique properties and the material's zero band gap respectively [3-4].

Among the number of investigated solutions, carbon nanotubes (CNTs) are the promising material [2]. Specifically, in the form of understanding the device physics and improving device performance for carbon nanotube field effect transistors (CNTFET) [5-8].

Since the first reports of single-walled carbon Nanotube (CNTs) in 1993 [9], they have been the subject of intense interest for basic and applied research. In CNTFET, ballistic or near-ballistic transport phenomena have been observed [10-11], and the existing design

infrastructure and fabrication process of CMOS-based MOSFETs can be also used for CNTFETs [12-14].

For low-power or low-voltage application such as laptop computers, mobile phone, and digital camera, the threshold voltage must be much smaller because of the use of ultra-low supply voltage there is a general consensus that V_T of the MOS devices in an application should approximately equal to $0.2 \times V_{DD}$, that is, for $1 - V_{DD}$, V_T should be 0.2V. For high-speed operation, high supply will be used and that requires a larger V_T value [15]. From the application point of view, the temperature dependence of the electronic devices is important for application of electronic system in some extreme conditions such as furnace temperature control and aerospace applications where the temperature can be far beyond the nominal operation range [16].

Our work is based on a numerical simulation developed with non-equilibrium Green's function (NEGF) approach. We study the threshold voltage in CNTFET and its dependence on the Gate length, the variation effect of nanotube diameter [17], Oxide thickness and the source/drain doped.

Silicon dioxide (SiO_2) has been facing the scaling limitation due to direct tunneling current that limits low power application and reliability. Recently, many high-k materials such as HfO_2 ($k=16$), ZrO_2 ($k=25$), Ta_2O_5 ($k=50$), and TiO_2 ($k \approx 35-100$) [18-21] have been introduced as alternative gate dielectrics to overcome leakage current problem. To consider the benefits of high-k gate dielectrics and CNTFETs, in this paper we present also the effects of high-k gate dielectric on the variation of

the threshold voltage. All these numerical studies have been done at wide range of temperature varying from 77 K to 400 K.

2. CNTFET Structure

A schematic cross-sectional is shown in Fig. 1(a) and 1(b). The source/drain length is 20 nm with heavily doped which is 10^9 nm^{-1} (~ 0.01 dopant/atom) and the channel is assumed intrinsic.

We study the variation of Threshold voltage (V_{TH}) when technological parameters are varying. Such as gate lengths (L_G), nanotube diameters (d), gate oxide thicknesses (t_{ox}), high-k gate dielectric constants and the source /drain doped.

The gate lengths of the CNTs used are 10nm, 15nm, 20nm, 25nm and 30nm. The chiralities used are (13,0), (16,0), (19,0), (23,0) and (25,0). The oxide thicknesses used are 1.5nm, 3nm, 4.5nm, 6nm and 7nm. In addition, the gate dielectric constants are 3.9, 16, 25, 50 and 80. These dielectric constants correspond to the dielectric constants for SiO_2 , HfO_2 , ZrO_2 , Ta_2O_5 , and TiO_2 respectively. And the source/drain doping used are 2.5 m^{-1} , 4 m^{-1} , 6 m^{-1} , 8 m^{-1} , and 10 m^{-1} (~ 0.01 dopant/atom).

For our simulations, we assume that the metal-Nanotubes contact resistance, $RC=0$, and carrier transport through Nanotubes is ballistic (no scattering). No gate-to-source or gate-to-drain overlap is assumed. The applied drain V_{DS} and gate V_{GS} biases vary from 0 V to 1 V. All calculations have been done at temperature ranging from 400 K down to 77 K.

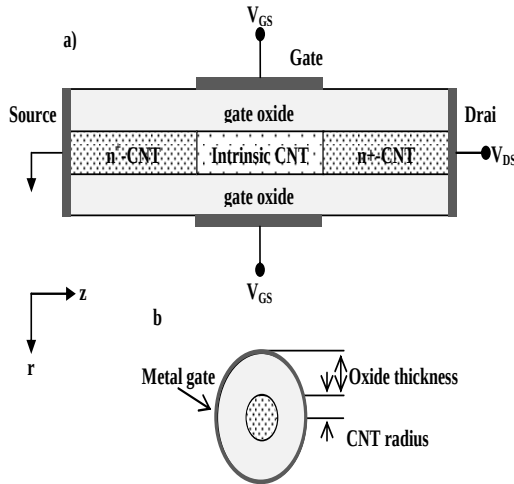


Figure 1. Symmetrical CNTFET considered in this work.

3. Simulated device

In order to simulate the proposed devices, a self-consistent solution of the Poisson and Schrödinger equations has been performed within the NEGF

formalism with a mode space approach presented in Ref. [19]-[22]. The NEGF method represents an ideal approach for nanoscale device simulations. In this approach, a nanoscale device is conceptually characterized by an active region connected to two large, in-equilibrium electron reservoirs (source and drain). Current flows as a result of an applied external bias between the source and drain which drives the system into a non-equilibrium state. Given the system Hamiltonian, the self-energy functions, and the contact electrochemical potentials, the NEGF approach is used to calculate the density matrix from which all other quantities of interest such as current are obtained [23].

The Poisson equation gives the electrostatic potential needed for calculating the Hamiltonian of the CNT. By solving the Schrödinger equation with the NEGF method, the density of states and the charge on the surface of the CNT is obtained. The new electrostatic potential is obtained through the use of the calculated charge and the solving of the Poisson equation using a 2-D finite difference method. The iteration between the Poisson and the Schrödinger equations continues until the self-consistency is achieved. Note that, ballistic transport was assumed.

It is convenient to solve Poisson's equations in cylindrical coordinates. Since the potential and charge are invariant around the nanotube, the Poisson equation is essentially a 2-D problem along the tube (z-direction) and the radial direction (r-direction) as Poisson equation is written as [24], [25]:

$$\nabla^2 V(r, z) = \frac{-q}{\epsilon} [p - n + N_D^+ - N_A^- + n_T] \quad (1)$$

Where $V(r, z)$ the electrostatic potential, q is the magnitude of the electronic charge, ϵ is the dielectric constant, p and n are the hole and electron densities, respectively, N_D^+ is the concentration of ionized donors, N_A^- is the concentration of ionized acceptors, and n_T is the fixed charge. The fixed charge is an input to the model and will be set to zero. The electron and hole concentrations (n and p , respectively) are computed by solving the Schrödinger equation with open boundary conditions by means of the NEGF formalism.

To calculate the Green's function for the device at a specific energy E , the following formula has been utilized [24]:

$$G(E) = [EI - H - \Sigma_S - \Sigma_D]^{-1} \quad (2)$$

Where 'I' is the identity matrix and 'H' is the Hamiltonian of the CNT, Σ_S and Σ_D are the self-energies for source and drain contacts, respectively.

The electron density is computed from the density of states (DOS), derived by the NEGF formalism. It can be calculated as follows:

$$n = \int_{E_i}^{+\infty} [D_S f(E - E_{FS}) + D_D f(E - E_{FD})] dE \quad (3)$$

Where E_i is the Fermi level within the CNT, $f(E)$ is the Fermi-Dirac distribution, and D_S (D_D), E_{FS} (E_{FD}) are the density of states and the Fermi energies of the source

(drain), respectively. A similar expression applies for holes. Once, self-consistency is obtained, the source-drain current can be expressed as

$$I = \frac{4q}{h} \int T(E)[f(E - E_{FS}) - f(E - E_{FD})]dE \quad (4)$$

Where h is Planck's constant and $T(E)$ is the transmission coefficient calculated by the NEGF formalism [26].

4. Simulation analysis and results

In this section, we present a description of the result obtained from the simulation which relates to the influence of gate length, nanotube diameter, oxide thickness, gate dielectric permittivity and channel doping on the threshold voltage (V_{TH}) behaviors.

First, to check the accuracy of our numerical calculations in the NEGF formalism for short channel devices, the drain current was calculated and compared with results obtained using the FETToy numerical model. Good agreement has been found [20]. It should be noted that the NEGF is an accurate quantum transport method intended to study the devices in the nanoscale regime.

Figure 2 illustrates the variation of V_{TH} as a function of gate length at different temperatures.

We notice that the threshold voltage (V_{TH}) is proportional to gate length (L_G) and decreases with increase of the (L_G).

A V_{TH} shift, which is due to diminution of temperature from 400 K to 77 K, can be easily observed (inset figure 2).

A maximum shift (about 0.415 V) is observed at low temperature 77 K

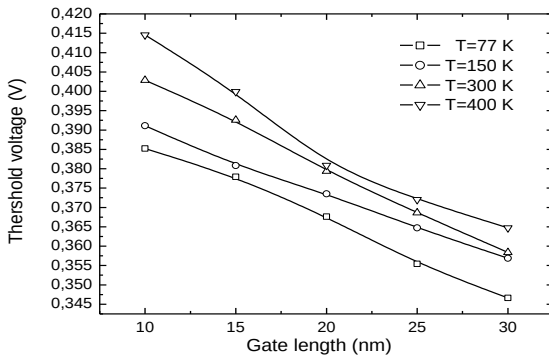


Figure 2. Threshold voltage versus gate length for various temperatures

Since the drain current depends on the nanotube diameter, the threshold voltage (V_{TH}) of the CNTFET should also be nanotube diameter dependent.

Figure 3 shows the threshold voltage as a function of the nanotube diameter for different temperatures.

It can be seen that when the nanotube diameter increases, V_{TH} decreases whatever the applied temperature. Therefore, CNTFETs turn ON at different gate voltages depending on their nanotube diameter.

This property will strongly influence the behavior of any logic gate based on CNTFETs. For investigating the impact of temperature on CNTFETs, we have changed the temperature from $T=400$ K down to 77 K and we have simulated the transistor behavior in this temperature interval.

Our results show that the decrease in temperature results in higher threshold voltage. A V_{TH} shift (about 42%) when T changes from $T=400$ K down to 77 K can be easily observed.

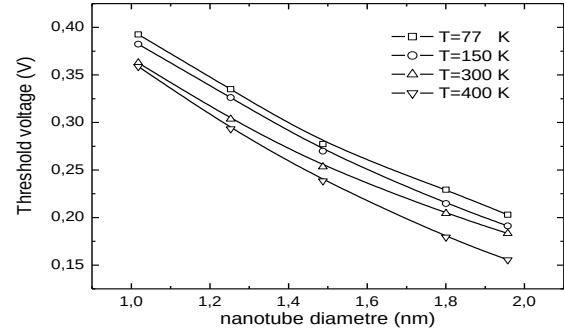


Figure 3. Threshold voltage versus nanotube diameter for various temperatures

Figure 4 represents the evolution of threshold voltage (V_{TH}) as a function of oxide thickness for different temperature varying from 77 K to 400 K. It can be observed that when oxide thickness increases, (V_{TH}) increases. In addition, one notes a reduction around 41.8% of V_{TH} when temperature varies from 400 K down to 77 K and this reduction remain practically feasible for all oxide thickness.

Silicon oxide (SiO_2) has been used as gate dielectric, since the inception of MOSFET in 1960, because of its electrical stability interface between Si and SiO_2 and thermal stability. When the gate dielectric is so thin, especially when it is less than 1.5 nm. Gate leakage due to direct tunneling of electrons through the SiO_2 will be too high, and circuit power dissipation will increase to an unacceptable value [19]. To overcome this problem the possible solution is to incorporate the use of a High-K gate dielectric. Figure 5, shows the threshold voltage against High-K materials of CNTFET device at different temperatures. High value of dielectric constant (K_{ox}) is not good for the threshold voltage (V_{TH}) of the device. The reason for such results can be clearly understood if we look at Eq. (5), which shows a direct relationship of gate capacitance with K_{ox} . Higher the value of K_{ox} the higher will be the CG and hence reduced V_{TH} .

$$C_G = \frac{2\pi K_{ox} \epsilon_0}{\ln\left(\frac{2T_{ox}}{d}\right)} \quad (5)$$

We have observed a higher threshold voltage in CNTFET with relatively lower K_{ox} material such as silicon dioxide and hafnium oxide. However, for a particular fixed drain current, the requirement of drain voltage is very low when High-K dielectric materials are used.

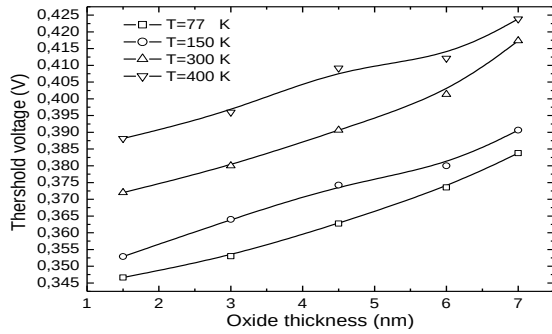


Figure4. Threshold voltage as function of oxide thickness at different temperatures.

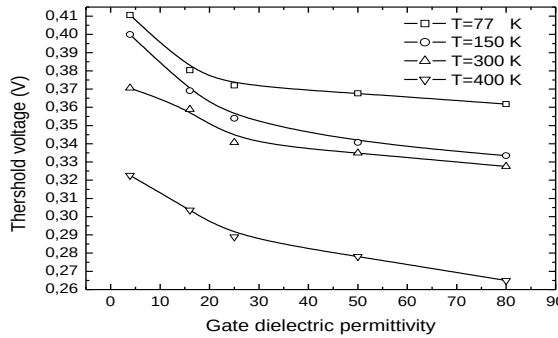


Figure 5. Threshold voltage variations with the gate dielectric permittivity at different temperatures

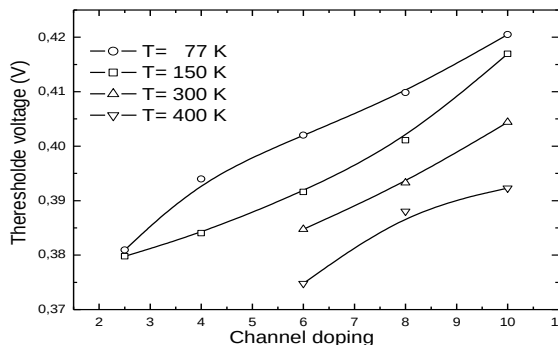


Figure 6. The effect of the channel doping in an CNTFET transistor on the threshold voltage is studied for different temperatures.

To enhance the performance of CNTFETs, advanced carbon nanotube field-effect transistors have been demonstrated with introduction of dopant in the channel. VLSI compatible doping technique [27], electronic and electrochemical doping [28] can make effective n- or p-type CNTFETs.

Figure 6 shows that the threshold voltage (V_{TH}) is proportional to channel doping. When channel dopings is raised, (V_{TH}) increases.

Noting that when channel doping varied between 2.5 m-1 and 6 m-1 for $T=300$ K and $T= 400$ K our program diverged and we can't get results.

As we can see from the same figure that the increasing in temperature results in lower threshold voltage. A V_{TH}

shift (about 40.5%) when T changes from $T= 400$ K down to 77 K can be easily observed.

Table 1, shows the variations in threshold voltage shift at different fixed temperatures.

It is very much clear that in CNTFET device, as the value of High-K materials increases, the threshold voltage shift remains constant around 86 mV.

Table1: Variation of average V_{TH} shift.

	Average V_{TH} shift $\Delta V_{TH} = V_{TH}(400 \text{ K}) - V_{TH}(77 \text{ K})$ [mV]
Effect of l_g on V_{TH} shift	19.6
Effect of ϕ on V_{TH} shift	42
Effect of t_{ox} on V_{TH} shift	41.8
Effect of K_{ox} on V_{TH} shift	86.8
Effect of channel doping on V_{TH} shift	40.5

5. Conclusion

In this study, we investigated the impact of different parameters on the threshold voltage of CNTFET in the nano-scale regime, using the non-equilibrium Green function (NEGF) formalism. Key settings of transistors; gate length, nanotube diameter, the oxide thickness, permittivity gate dielectric and the channel doping were studied. it is found that the threshold voltage (V_{TH}) decreases as the oxide thickness and the channel doping decrease. we also found that V_{TH} reduced where the temperatures vary from 400K down to 77K. In addition, as the gate length, the nanotube diameter and the gate dielectric permittivity augment the threshold voltage (V_{TH}) decreases.

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